REMARKS

Claims 1, 2, 5-14, and 16 have been rejected under 35 USC 102(e) as being anticipated by Brigham et al. (2001/0036693). Claim 15 has been rejected under 35 USC 103(a) as being unpatentable over Brigham. Claims 3 and 4 have been indicated as containing allowable subject matter. Claims 17-25 have been withdrawn from consideration.

In rejecting the claims, the Examiner states the following:

> ... Brigham teaches the inventive structure, for example as shown in Fig. 9, with a fin field effect transistor having a fin (104) above the substrate, source/drain regions (114) outside the fin and above the substrate, a gate (120) along the fin, and a diffusion barrier (112) situated between the source/drain regions and the fin, and where the fin acts as the channel between the source and drain, as claimed.

Claim 1 has been amended to recite "an insulator layer on the substrate." Support for this feature can be found in paragraph 0068 of the application where it states that "(t)he fin field effect transistor 100 is designed as an SOI structure (SOI: Silicon on Isolator). In this case, the structure is constructed on the insulation layer of a wafer."

Fig. 1 of the application clearly shows the insulating layer formed in the form of an oxide layer 102. In contrast, as can be seen from Fig. 9 of Brigham et al., there is no insulator layer separating the substrate 102 from the fin or pillar 104. In fact, the pillar 104 is a part of the substrate 102. (See, for example, paragraph 0039 of Brigham et al. stating that "substrate 102 has one or more pillars 104.")

Paragraph 0023 of Brigham et al. discusses the various previous attempts of reducing parasitic junction capacitance, stating:

> The speed and power performance characteristics of MOSFET integrated circuits can be improved by reducing parasitic junction capacitance. Various attempts to reduce this junction capacitance have included fabricating transistors on insulating substrates, for example sapphire, or more commonly, a **silicon-on-insulator (SOI) substrate**. While these approaches do reduce the junction capacitance associated with FET structures by isolating the junctions from the

semiconductor body, unfortunately they also create device performance problems due to the floating body effect.

(Emphasis added.)

Consequently a different approach is used and disclosed in Brigham et al., which does not use an insulator layer on the substrate.

Therefore, not only does Brigham et al. not anticipate the present invention as recited in claim 1, but also expressly teaches away from the invention.

On page 3 of the Office Action, the Examiner objected to claims 3 and 4 as being dependent upon a rejected base claim, but stated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Therefore, Applicant has added new independent claim 26, having all the features of original claims 1 and 3, and new dependent claim 27 having the features of original claim 4. New claims 26 and 27 should therefore be allowable.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By Laura C. Brutman

Laura C. Brutman
Registration No.: 38,395
DARBY & DARBY P.C.
P.O. Box 5257
New York, New York 10150-5257
(212) 527-7700
(212) 527-7701 (Fax)
Attorneys/Agents For Applicant